

FORM PTO-1449 (Modified)

ATTY. DOCKET NO.:
YOR919980370US1

SERIAL NO.: 09/239,323

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S
INFORMATION
DISCLOSURE STATEMENT

APPLICANT: Jenkins et al.

(Use several sheets if necessary)

FILING DATE: 01/28/99

GROUP: 2871

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

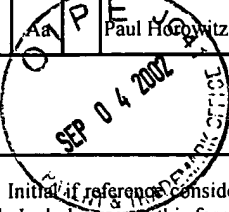
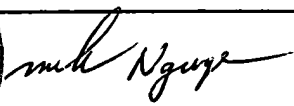
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
VN	AA 5 1 3 6 6 2 2	8/4/92	Plus	377	64	
	AB 5 1 4 8 0 5 8	9/15/92	Stewart	307	453	
	AC 5 2 2 4 1 0 2	6/29/93	Plus et al	371	21	
	AD 5 6 1 9 2 2 3	4/8/97	Lee et al.	345	93	
	AE 5 1 7 0 1 5 5	12/8/92	Plus et al.	340	784	
	AF 5 1 7 5 4 4 6	12/29/92	Stewart	307	463	
	AG 5 2 2 2 0 8 2	6/22/93	Plus	377	79	
	AH 5 4 1 0 5 8 3	4/25/95	Weisbrod et al.	377	75	
	AI 5 6 5 4 9 7 0	8/5/97	DaCosta et al.	371	22	
	AJ 5 1 6 6 9 6 0	11/24/92	DaCosta et al.	377	70	
	AK 5 5 7 6 7 3 0	11/19/96	Shimada et al	345	98	
	AL 5 5 3 9 3 2 6	7/23/96	Takahashi et al	324	770	
	AM 5 4 6 5 0 5 3	11/7/95	Edwards	324	770	
	AN 5 5 4 6 0 1 3	8/13/96	Ichioaka et al	324	770	
	AO 5 5 0 6 5 1 6	4/9/96	Yamashita et al	324	770	
	AP 5 1 7 9 3 4 5	1/12/93	Jenkins et al	324	678	
↓	AQ 6 4 3 7 5 9 6	8/20/02	Jenkins et al.	324	770	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
						YES NO
VN	AR 5 7 0 1 1 5 B1	8/19/98	European Patent Office			
VN	AS 5 7 0 1 1 5 A3	11/18/93	European Patent Office			
VN	AT 5 7 0 1 1 5 A2	11/18/93	European Patent Office			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

VN	AU	Fryer, et al., "A Six Mask TFT/LCD Process Using Copper Gate Metallurgy", IBM Research Report, RC 20594, October, 1996.
VN	AV	Colgan et al., "A 10.5-in.-diagonal SXGA active-matrix display," IBM Journal of Research and Development, Vol. 42, No. 3/4, May/July 1998, pp. 427-444
VN	AW	Arai et al., "Aluminum-based gate structure for active-matrix liquid crystal displays," IBM Journal of Research and Development, Vol. 42, No. 3/4, May/July 1998, pp. 491-499.

VN	AX	L.C. Jenkins et al., "Function Testing of TFT/LCD arrays" IBM Journal of Research and Development vol. 36, No.1, Jan. 1992 pp. 59-68.
VN	AY	S. Kimura et al., "High-Speed Testing of TFT-LCD Array" Society for Information Displays International Symposium Digest of Technical Papers, Vol. 23, 1992, pp. 628-631.
VN	AZ	R.L. Wisnieff et al., "In-Process Testing of Thin-Film Transistor Arrays" Society for Information Displays International Symposium Digest of Technical Papers, Vol. 21, 1990, pp. 190-193.
VN	AA	Paul Horowitz et al., "The Art of Electronics" Cambridge University Press (1980) pp. 242-247, 334-338.
EXAMINER	 	
DATE CONSIDERED		08/20/03
EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		

RECEIVED
 SEP - 6 2002
 TECHNOLOGY CENTER 2800